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HOCHSCHULE PFORZHEIM

Workshop on Xilinx FPGA for video processing

Accelerate the design through Digilent ZYBO & Vivado HLS

SEPTEMBER 12, 9AM TO 2PM

HOCHSCHULE PFORZHEIM

Learn Basics of High Level Synthesis for FPGAs and Real-time Video Processing pipelines.

Understand the viability of video processing in reprogrammable logic instead of software running on a general purpose microprocessor.

Presented by: Elod Gyorgy, Senior Engineer, Digilent Inc.

Co-Sponsored by: trenz electronic

Workshop on Xilinx FPGA for real-time video processing

Accelerate the design through Digilent ZYBO & Vivado HLS

Presenter: Elod Gyorgy

Event Organizer: Digilent Inc, Trenz, Hochschule Pforzheim

Goals of the Workshop:

1) Introduce participants to the basics of High Level Synthesis for FPGAs and Real-time Video Processing pipelines. Illustrate the viability of video processing in reprogrammable logic instead of software running on a general purpose microprocessor.

2) Demonstrate the ease of use of Digilent Video Processing Platforms.

3) Show how Digilent freely available Intellectual Property modules can be (re)used in customer projects.

Description: The workshops keeps in line with Digilent's mission of providing hands-on, project-based, open-ended approach to education. The Zybo allows every participant to implement a real-time video processing platform and visualize the results in hardware.

Zybo board from Digilent and the free WebPack version of Vivado HLS from Xilinx expose students to the newest technologies both in hardware and software. The examples will use VHDL and C++ language and will demonstrate HLS design flow, IP core usage, simulation and HW debugging.

Preferred time: September 12, 2017 9AM-2PM 20+ attendees

Qualifications of Presenter:

Elod GYORGY is a Digital Design Engineer with over 8 years of experience in Xilinx FPGA technologies and embedded software development. Currently, he works at the Romanian branch of Digilent Inc., a leading electrical engineering products company serving students and universities with education design tools.

Audience: The anticipated audience includes faculty members, instructors, and laboratory staff in Electrical and Computer Engineering and Engineering Technology, Mechanical Engineering and Engineering Technology, First Year Engineering Education, Engineering Physics, Physics, and middle and high school teachers in the physical sciences. Participants need to have basic knowledge about VHDL, C/C++ and digital design. They will leave the workshop with instructional materials so that participants can easily adopt this innovative technique in their own courses.

The workshop will be held in English.

Take-Away Skill, Knowledge, and Material: Participants will learn about the active hands-on learning pedagogy, see how others have integrated hands-on learning modules into the engineering and engineering technology courses, and labs and suggestions on ways in which the participants can adapt the pedagogical approach for their use. Flash drives will be distributed that will include the workshop presentation.

Logistics:

Digilent will bring 20 Zybo boards + USB a to Micro B cables. No HW donation during the workshop.

Venue: - make sure that there are 20 computers available, projector and screen available for the presenter.

Computers should have:

- Vivado 2015.4 HLx Webpack installed

- HDMI output with HDMI-to-HDMI cable OR DisplayPort++ output with DisplayPort-to-HDMI cable OR

DVI output with DVI-to-HDMI cable/adaptor

- monitor with VGA input and VGA cable