Hochschule Reutlingen
Reutlingen University

Design of an ASIC for Sensorless Control of a Switched Reluctance Motor

Erik John, Till Moldenhauer, Lukas Riedel, Zong Xern Sim, Eckhard Hennig

***Abstract*—Switched Reluctance Motor (SRM) drives have gained interests over the last few years due to being low-cost and robust as well as not utilizing permanent magnets. However, the control schemes necessary for SRMs typically require expensive hardware and complex software. A recent novel control scheme overcomes these problems by injecting a current additionally in another phase and evaluating the corresponding current controller's PWM frequency by digital logic gates. The work in this paper adapts and expands this idea by implementing this method in an application-specific integrated circuit (ASIC) in a 350 nm technology for further reducing system cost as well as increasing portability. The ASIC integrates three main functionalities necessary for motor control: phase sequencing, current control and position detection. Full performance is achieved in simulations but also in the laboratory on real hardware at least up to 5800 revolutions per minute on a DC link voltage of 325 V. In conclusion the developed ASIC is the first of its kind and allows system designers to implement a SRM motor control faster and thereby spreading the application range.**

***Index Terms*—Switched Reluctance Motor, SRM, Motor Control, ASIC, Power Electronics**

I. Introduction

Switched reluctance motors are characterized by a cost-effective and robust construction due to not utilizing permanent magnets. Moreover, this is a benefit under the light of sustainability because the materials for permanent magnets are often mined noxiously. Therefore, SRMs offer a lot of potential in different product areas such as kitchen equipment or even in automotive applications. However, the control system needed for the application of SRMs typically consists of expensive hardware and/or complex software thereby reducing the system cost-effectiveness. One possibility to reduce costs is to control the SRM without position detection sensors, which is the area of interest for this paper. According to [5], three general sensorless control schemes can be currently identified:

1) *Observer based methods*
   In [7] the authors showcase a state observer derived from the linear state equation. The work in [9] exploits the nonlinear relationship between flux linkage, current and rotor position while implementing a sliding mode position observer. Observer based methods are typically characterized by the necessary non-negligible computational power [5].
2) *Incremental inductance based methods*
   These methods rely on the fact that the incremental inductance is proportional to the phase current rise and fall times. From that the rotor position can be derived [5]. Recent research in this area is presented in [4], where a digital signal processor is used for motor control.
3) *Direct inductance based methods*
   The third method of controlling a SRM makes use of observing the motor inductance. The inductance and, consequently, the rotor position is determined by evaluating the current signal.
   The work described in [1] deals with the injection of a DC pulse into an unused phase to determine the phase inductance. By processing an inductance vector, which is set up using a Clark transformation, in a PLL, the rotor position and speed can be calculated.
   The method in [3] is based on the measurement and comparison of two consecutive switch-on times. The approach is characterised by its simplicity and resistance to disturbances in dynamic operation.

The novel control algorithm proposed in [11] utilizes simple digital logic components to estimate the rotor position based on the switching frequency of the hysteresis phase current controller. Besides the suitability of this algorithm to be implemented in an ASIC, there is also no other integrated circuit (IC) currently available in the market for SRM control. In [6] and [2], SRM control ASICs are described, but in contrast to ASIC presented in this paper, they do not feature internal rotor position detection and rely on external position sensors. Consequently, the proposed SRM control ASIC could contribute to reducing system costs and development resources for this motor and, thus, to extending the application range.

Erik John, erik.john@student.reutlingen-university.de, Till Moldenhauer, till.moldenhauer@student.reutlingen-university.de, Lukas Riedel, lukas.riedel@student.reutlingen-university.de, Zong Xern Sim, zong_xern.sim@student.reutlingen-university.de, Eckhard Hennig, eckhard.hennig@reutlingen-university.de. Reutlingen University, Alteburgstraße 150, 72762 Reutlingen.

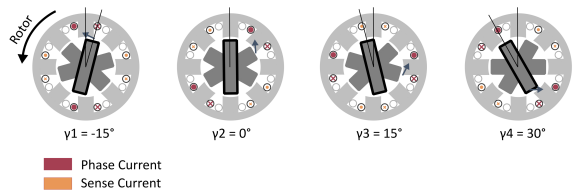

Figure 1. SRM working principle

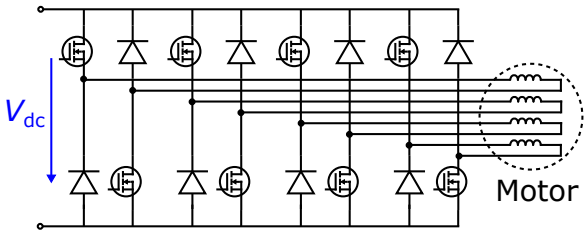

Figure 2. Asymmetric half-bridge

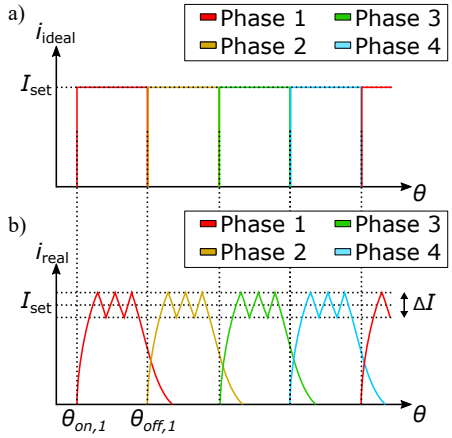

Figure 3. Current signals

II. Theoretical Background

A. General operation of a SRM

The torque generation in SRMs can be derived from the tendency of a magnetic circuit to assume its state of minimal reluctance. In a SRM, the rotor consists of discrete poles and, thereby, variable reluctance in the active magnetic circuit when spinning. The stator is composed of distinct coil halves in opposition to each other, which form the active magnetic circuit when current is flowing through that coil. As shown in Figure 1, the rotor pole most closely to the active stator coil (Red) aligns itself. A continuous rotation can be achieved by switching between the coils periodically, where the correct timing is of crucial importance [8].

B. The power electronic circuit

As already indicated in Section II-A, the torque is generated by driving current through the stator coils.

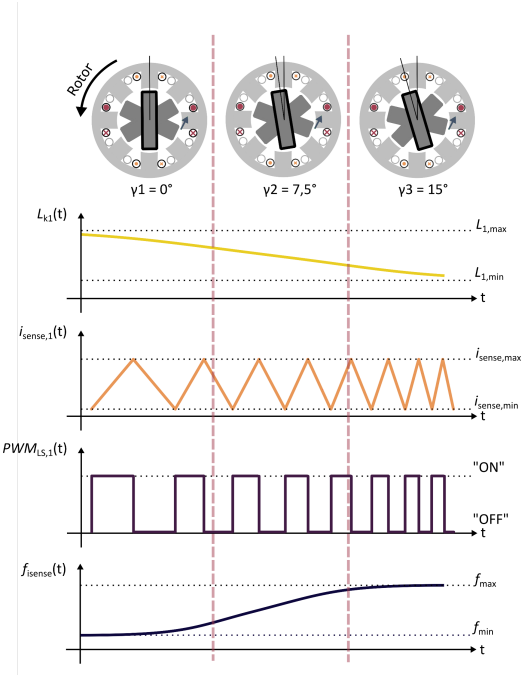

Figure 4. Connection between switching frequency and rotor position

The typical circuit to fulfill this task is called the asymmetric half-bridge, shown in Figure 2. With this circuit configuration, it is possible to drive nearly ideal block currents through the coil. Due to the inductance of the motor, though, the real current signals feature slopes and a hysteresis around the setpoint (see Figure 3). Fast demagnetization can be achieved by turning off both switches on one of the coils so that the negative DC link voltage occurs across that coil. The current is typically controlled via PWM signals with variable frequency [8].

C. The novel sensorless method for SRM control

The variable inductance when rotating leads to rising and falling PWM frequencies, from which the time instants for switching phases can be derived.

The authors of [11] recognized that using the torque generating coil for position sensing also does not lead to robust results, especially in higher speed modes. Therefore, they propose to use one of the inactive phases as the rotor position sensing coil by driving a small current through it. This can be seen in Figure 4. The reluctance of the torque generating coil (red) decreases and thereby its inductance increases while the rotor aligns itself. Contrary, the reluctance of the sensing phase (orange) increases and its inductance decreases because the rotor moves away. This movement can be seen in the rising PWM frequency of the sensing current controller. Utilizing the PWM signal and not the current itself facilitates the evaluation by simple digital hardware. The pairing of torque generating and sensing phase is constant and chosen so that the

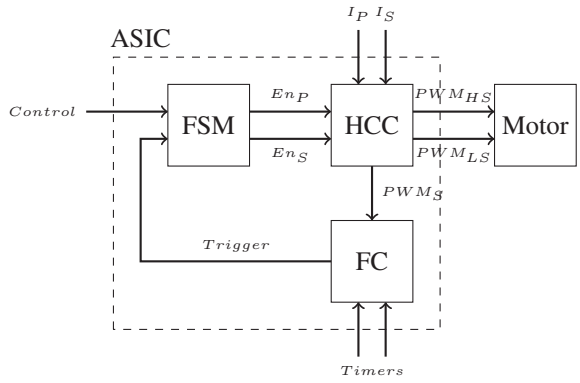

Figure 5. Block diagram

sensing phase is least aligned for the best position estimation. For the utilized SRM the phases 1 and 3 as well as 2 and 4 are paired alternating between power and sensing mode.

III. System Design

The method to develop the ASIC can be described as a top-down approach. Firstly, the partition of the motor control function into smaller sub-functions is done on system level resulting in a block diagram. Subsequently, the sub-functions are detailed, developed and simulated according to an analog and digital design flow. The design phase concludes with the verification of the parasitic extracted layout in simulations.

A. Project conditions

Besides the main requirement for the ASIC to control a SRM with eight stator teeth, the ASIC shall be able to work as a stand-alone system not needing any form of microprocessor or similiar for the basic operation. Moreover, the operation parameters such as the turning direction, the current setpoint values and frequency trigger points shall be configurable. Each main block shall be separately testable.

B. Block diagram

According to the technique to control the SRM in [11], there are three main functionalities, which must be handled by the ASIC:

- Determining the phases to be energized and their sequence.
- Controlling currents and generating the pulse signals for the asymmetrical half bridge.
- Detecting frequency thresholds that lead to phase current switching.

Therefore, as shown in the block diagram, three main modules are introduced (see Figure 5).

a) Finite state machine (FSM): Each of the four power states of the motor can be represented as part of a state transition diagram. In each state, the power phase and sensing phase are in a fixed local relationship to one another (see Chapter II-C). An internal trigger signal causes the state machine to change its state. External control signals can be used to start, stop and reset. Depending on the state of the machine, corresponding enable signals for the power phase and the sensing phase to be measured are passed on to the following block.

b) Hysteresis current control (HCC): Depending on an external current measurement in the powered motor phases, a current control is carried out in the chip. The current is controlled with a fixed hysteresis of $100\,\mathrm{mA}$ around the reference currents set for the power phase and sensing phase. For this purpose, the transistors of the asymmetrical half bridges are controlled with the PWM signals generated in the hysteresis controller. Within the ASIC, the PWM signals of the current controllers for the sensing phase are synthesized and transmitted to the third main module.

c) Frequency comparator (FC): To determine the right time for the phase change, the transmitted PWM signal of the sensing phase is monitored in this block. For this purpose, the time between two signal edges is measured and compared with a set timer value. If its frequency is greater than the upper hysteresis threshold, the internal trigger signal is set to low. This causes the state machine to switch to the next motor state. In order to use the ASIC for different motor inductances, voltages and speeds, the values of the timers can be changed individually.

The output signals of each of the three main components are connected to chip pads, so they can be monitored or replaced by external signals.

IV. Circuit Design and Simulation

The circuit design of the ASIC is divided into an analog and a digital workflow. While the analog design is only used for the hysteresis current controller, the digital workflow is applied for the other two main components, as well as some interconnection elements.

A. Analog design workflow

Each of the four half bridges has to be driven by one high side and one low side PWM signal to achieve the desired current flow with a hysteresis of $100\,\mathrm{mA}$. A Schmitt Trigger consisting of a comparator with two resistors serves this purpose. The hierarchical circuit is then implemented using XFAB's IP components. A functional schematic of the HCC of one phase is shown in Figure 6. The setup consists of two inverting Schmitt triggers per phase, which are connected via various logic gates to generate the required PWM signals of the high and low side.

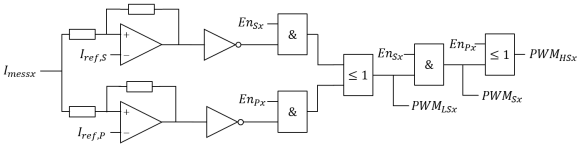

Figure 6. Schematic HCC for one phase

B. Digital design workflow

The digital circuitry is controlled by a 1 MHz clock providing marginal angle error with respect to the SRM's expected maximum speed. The digital circuits are described in the hardware description language VHDL and synthesized as a digital circuit using the Cadence Genus tool.
As shown in Chapter III, the logic to control the phase activation and sequencing can be described as a Moore machine. The FC is implemented using timers to measure the time between two rising PWM edges. Furthermore smaller logic circuits are responsible for blending the four PWM signals for each halfbridge into one glitch free signal as the FC's input. All distinct blocks are connected with each other on a top level description forming one monolithic digital design.

C. System simulation

In order to be able to carry out the simulations to prove the correct functions of all components in the ASIC, a motor model must be built that corresponds to the SRM's behaviour (Figure 7). This is done by qualitatively describing the SRM's angle-dependent inductance in VHDL-AMS by a hyperbolic function.
The equation for the angle dependent inductance is:

$$L = L_{amp} \cdot (1.0 + \tanh(a \cdot \cos(\alpha \cdot \Theta \cdot b))) + L_{min}$$

with
$\alpha = konst. = \frac{T \cdot \pi}{180°}$
$L_{amp} = konst. = 0.5 \cdot (L_{max} - L_{min})$
a: Slope steepness
b: Phase shift
Θ: Rotation angle

Figure 8 shows the resulting inductance. The modelled inductance curves deviate from the real ones at the top, but for the intended simulations only the inductance range, the slope steepness as well as the relative value to each other (crossing points) are relevant. Hence, the qualitative model meets these requirements and is appropriate for the intended application.
Consequently, all the resulting function groups are combined with the motor model into one system simulation model. The simulation of the start-up and operating behaviour provides the results shown in Figure 9.
Initially, no phase is energized. When the system is enabled, phases 1 and 3 are used to align the motor and

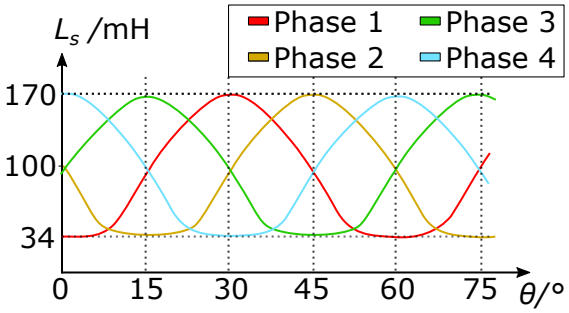

Figure 7. Real inductance curve [10]

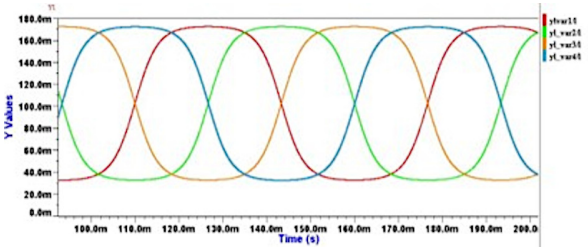

Figure 8. Modelled inductance curve

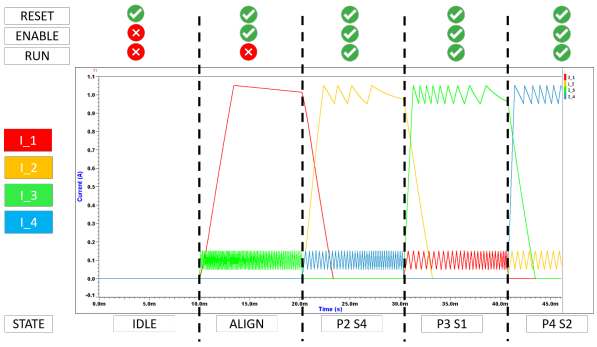

Figure 9. System simulation result

put it in a defined state. The motor can start from this state. Subsequently, the current control is successfully carried out in all phases and the frequency thresholds are detected in the sensing phase, so that a phase change occurs.

V. Layout Design and Verification

The ASIC has been designed and fabricated in XFAB's XH035 350 nm CMOS process with three metal layers. The chip area is 2158 µm x 1880 µm and the Cadence Virtuoso view is displayed in Figure 10.
The core design constitutes the center part of the ASIC whereas the ESD frame forms the outer boundary. Between those two instances buffer capacitors have been placed. The core design's bottom part is formed by the digital circuitry. The digital layout is implemented using the Cadence Innovus toolchain. On the left hand side one can find the ADCs used to set the frequency comparator limits as IP blocks. On the

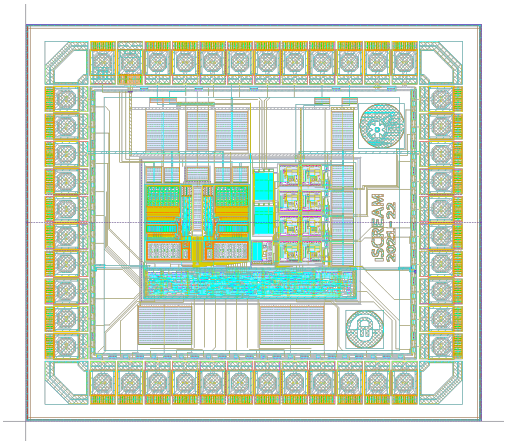

Figure 10. ASIC physical design

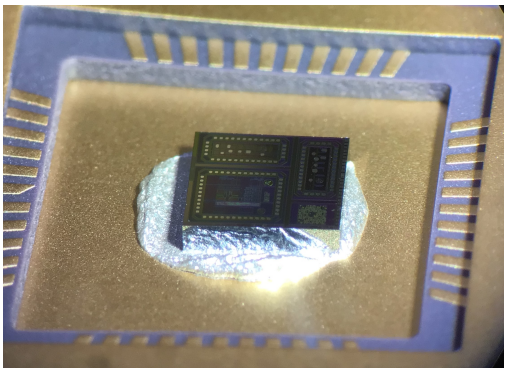

Figure 11. Manufactured die with the SRM control ASIC design in the bottom left corner

right hand side there are the current controller circuits with comparator IP blocks.

During the layout phase, specific attention has been laid upon achieving a compact floorplan, short trace lengths as well as matching similar components to gain robustness against production tolerances and other external influences. The ASIC design presented in this paper has been placed on one die with other chip designs. The result after manufacturing and before bonding can be seen in Figure 11.

VI. Commissioning

The main functionality of the ASIC is to control a system which can drive a SRM. For this purpose, the ASIC is placed in a suitable power electronics system consisting of multiple printed circuit boards (PCBs) displayed in Figure 12. Via gate driver ICs, the ASIC's output signals control four asymmetric half bridges connected to the SRM's stator coils. The current is sensed by hall effect sensors delivering a corresponding signal to the ASIC. Low interference on the analog signals as well as secure transmission of the control signals is crucial for the functionality.

Figure 13 shows the results of the ASIC's successful operation. The purple signal represents the PWM_C

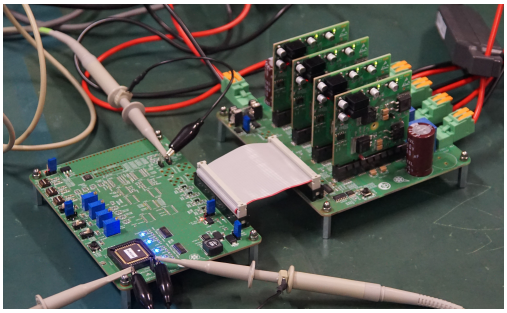

Figure 12. ASIC in the power electronic system

signal resulting from the merger of the four PWM signals (one for each half bridge) into one signal which is fed to the FC. The pink signal ($Trig$) is the output of the FC, indicating the moment in time to switch phases. With every rising edge of the brown signal (RPM), one complete cycle through the state machine is finished. This documents the correct cycling. The four current signals on the top of Figure 13 display the two possible alternating states of the motor phases. When used in power mode, the current does not reach its maximum due to the low DC bus voltage and, therefore, no hysteresis can be seen. When used in sense mode, the hysteresis is clearly visible, proving the correct functionality of the hysteresis current controller inside the ASIC. Moreover the pairing of phase 1 and 3 as well as 2 and 4 becomes apparent. The increased noise in phases 2 and 4 is due to the measurement by current clamps with different resolutions.

VII. Conclusion

This paper shows the possibility to put a sensorless control algorithm into an ASIC, which can be used with a variety of 8/6 SRMs because of the configurability via analog input signals. The ability to control a SRM supplied with mains voltage makes the ASIC suitable for real world applications. Due to facilitating the application of this motor type by integrating several functions necessary for motor control designers do not have to think about those anymore. The described functions comprise position detection and current control but not the speed control. Therefore further work on this chip could mean implementing speed control and initial position detection. Furthermore the ability to work not only with 8/6 SRMs but other motor setups could be included.

VIII. Acknowledgement

The work displayed in this paper has been generously financed by the MPC group and the authors would like to express their gratitude here.

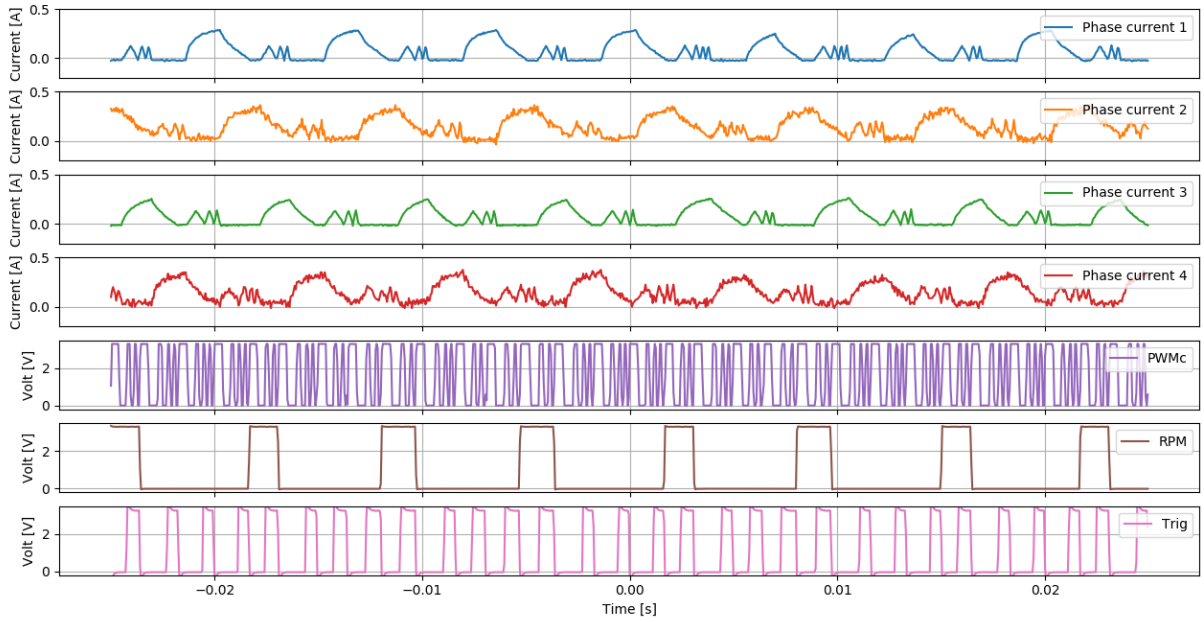

Figure 13. ASIC performance proven in the laboratory

References

[1] Alecksey Anuchin u. a. „Self-sensing Control of a Switched Reluctance Drive Using Voltage Pulse Injection“. In: *2018 X International Conference on Electrical Power Drive Systems (ICEPDS)*. IEEE, Dez. 2018. DOI: 10.1109/ICEPDS.2018.8571654.

[2] Hai-Jin Chen, Sheng-Li Lu und Long-Xing Shi. „Development and validation of a general-purpose ASIC chip for the control of switched reluctance machines“. In: *Energy Conversion and Management* 50.3 (März 2009), S. 592–599. DOI: 10.1016/j.enconman.2008.10.013. URL: https://doi.org/10.1016/j.enconman.2008.10.013.

[3] Jaehyuck Kim, Hyong Yeol Yang und R. Krishnan. „Parameter Insensitive Sensorless Control of Single Controllable-Switch-Based Switched Reluctance Motor Drive“. In: *8th International Conference on Power Electronics - ECCE Asia*. IEEE, Dez. 2011. DOI: 10.1109/ICPE.2011.5944561.

[4] Jongwan Kim und Jih-Sheng Lai. „Quad Sampling Incremental Inductance Measurement Through Current Loop for Switched Reluctance Motor“. In: *IEEE Transactions on Instrumentation and Measurement* 69.7 (2020), S. 4251–4257. DOI: 10.1109/TIM.2019.2949319.

[5] R. Krishnan. *Switched Reluctance Motor Drives - Modeling, Simulation, Analysis, Design, and Applications*. Boca Raton, Fla: CRC Press, 2017. ISBN: 978-1-351-83595-4.

[6] T.J.E. Miller, C. Cossar und D. Anderson. „A new control IC for switched reluctance motor drives“. In: *1990 Fourth International Conference on Power Electronics and Variable-Speed Drives (Conf. Publ. No. 324)*. 1990, S. 331–335.

[7] Yoshihiro Nakazawa und Serina Matsunaga. „Position Sensorless Control of Switched Reluctance Motor Using State Observer“. In: *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*. 2019, S. 1–4. DOI: 10.1109/ICEMS.2019.8921668.

[8] Dierk Schröder und Joachim Böcker, Hrsg. *Elektrische Antriebe – Regelung von Antriebssystemen*. Springer Berlin Heidelberg, 2021. DOI: 10.1007/978-3-662-62700-6. URL: https://doi.org/10.1007/978-3-662-62700-6.

[9] Xiaodong Sun u. a. „Position Sensorless Control of Switched Reluctance Motor Drives Based on a New Sliding Mode Observer Using Fourier Flux Linkage Model“. In: *IEEE Transactions on Energy Conversion* 37.2 (2022), S. 978–988. DOI: 10.1109/TEC.2021.3125494.

[10] Annika Walz-Lange. „Entwicklung einer leistungselektronischen Baugruppe zur Ansteuerung einer geschalteten Reluktanzmaschine“. Bachelorthesis. Reutlingen University, 2020.

[11] Annika Walz-Lange und Gernot Schullerus. „Sensorless Control of a Switched Reluctance Machine Based on Switching Frequency Evaluation“. In: *2020 XI International Conference on Electrical Power Drive Systems (ICEPDS)*. IEEE, Okt. 2020. DOI: 10.1109/icepds47235.2020.9249339.

Erik John received his Bachelor degree in Electrical Engineering in 2021 from DHBW Stuttgart. Currently he pursues his Master degree in Power- and Microelectronics at Reutlingen University. Recent activities include among other things the ASIC development for switched reluctance motors.

Till Moldenhauer received his Bachelor degree in Electrical Engineering in 2019 from DHBW Stuttgart. Currently he pursues his Master degree in Power- and Microelectronics at Reutlingen University. Recent activities include among other things the ASIC development for switched reluctance motors.

Lukas Riedel received his Bachelor degree in Electrical Engineering in 2019 from DHBW Ravensburg. Currently he pursues his Master degree in Power- and Microelectronics at Reutlingen University. Recent activities include among other things the ASIC development for switched reluctance motors.

Zong Xern Sim received his Bachelor degree in Electrical Engineering in 2020 from Mannheim University of Applied Sciences. Currently he pursues his Master degree in Power- and Microelectronics at Reutlingen University. Recent activities include among other things the ASIC development for switched reluctance motors.

Eckhard Hennig received the Dipl.-Ing. degree in electrical engineering from the Technical University of Braunschweig, Germany, in 1994 and the Dr.-Ing. degree from the University of Kaiserlautern, Germany, in 2000. He is a Professor of digital and integrated circuits with Reutlingen University, Germany. His research interests include low-power CMOS circuit design for smart-sensor applications and electronic design automation.